TURBO-CODE DECODER

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention generally relates to a decoder, and more particularly, to a fast turbo-code decoder. The decoder is designed to use the systolic array very large scaled integrated (VLSI) circuits; the output of previous level can be used as the input of next level. Thus, the advantages of the parallel and the pipeline calculation are totally achieved. The decoding speed has improved manifestly comparing to the calculation time of the conventional decoder. The speed has about 5*(N+M) times faster than the conventional decoder, wherein, N stands for the block length, and M stands for register size.

Description of Related Art

[0002] The error control coding is widely used in the communication system and the computer media storage. Berrou, Glavieux and Thitimajshima first proposed the turbo-code whose error-correcting capability nears to the Shannon limited error-correcting in 1993 (C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon Limited Error-correcting Coding and Decoding: Turbo-codes (1)," in Proc. ICC'93, May, 1993). Since the excellence of the error-correcting capability, the turbo-code is widely applied in the general communication system such as the CDMA transmission system. Whereas, if the block length of the conventional decoding algorithm is too small, the error-correcting capability is not good, wherein the block length is for transmission. On the other hand, if the block length of transmission is too large, for a communication system needs the real time processing, the decoding delay is too large to tolerant. Therefore, it is important to solve this problem to fulfill the requirement of the current high-speed communication.

SUMMARY OF THE INVENTION

[0003] To solve the problem mentioned above and to increase the computing speed and thus to increase the throughput. The present invention provides a structure design using the parallel and systolic array VLSI.

[0004] The structure design adopting the parallel and systolic array VLSI mentioned above, wherein the decoder is designed to use the systolic array VLSI circuits. Since the output of previous level can be used as the input of next level. So the advantages of the parallel and the pipeline calculation are totally achieved. The latency is only N+M+2 units of time, the latency is shorten to as about 1/5 comparing to the conventional sequential calculation structure that takes 5*(N+M) units of time. The decoding throughput is about 5*(N+M) times higher than the conventional decoder. Although the quantity of the circuit gate is about 5*(N+M) times higher than the conventional decoder. However, the VLSI techniques had been progressively improved nowadays, thus the hardware complexity is easy to overcome. Devoting the hardware cost to get the higher speed will be a changeless trend.

[0005] In order to achieve the objective mentioned above, the present invention uses a parallel and systolic array VLSI structure design to provide a turbo-code decoder for the communication system. The decoder comprises a serial-to-parallel output unit and a plurality of parallel decoding units. Wherein, the serial-to-parallel output unit receives a serial input signal, converts it and outputs a parallel signal. The parallel decoding units mentioned above are serially connected to form a plurality of levels. The first level parallel decoding unit receives the parallel signal that is output from the serial-to-parallel output unit. The output from the first level parallel decoding unit is sent to the second level parallel decoding unit, with certain sequence, the parallel signal passes through the parallel decoding units for decoding process.

[0006] The turbo-code decoder mentioned above, wherein, each parallel decoding unit receives an extrinsic parameter when processing the decoding process, to be the signal that is after the decoding process from the parallel decoding unit, and sends the extrinsic parameter to the next level of the parallel decoding unit.

[0007] The turbo-code decoder mentioned above, wherein, the extrinsic parameter is obtained from a deinterleaving operation. The extrinsic parameter of the first level parallel decoding unit is $L_{a0,k}$=(0,0...,0), where k=1, 2, ..., N, N is the block length of the turbo-code.

[0008] The turbo-code decoder mentioned above, wherein, the serial input signals are $r_{1s,k}$, $r_{1p,k}$, and $r_{2p,k}$ messages of the turbo-code, whereas k=1, 2, ..., N, N is the block length of the turbo-code.

[0009] The turbo-code decoder mentioned above, wherein, the serial-to-parallel output unit receives the $r_{1s,k}$, $r_{1p,k}$, and $r_{2p,k}$, wherein, the subscript K=0, 1, ..., N+M-1 represents the whole block and end message. M stands for register size of the turbo-code decoder. The serial-to-parallel output unit coverts the received $r_{1s,k}$, $r_{1p,k}$, and $r_{2p,k}$ messages and outputs the results to the first level parallel decoding unit in parallel. The first level parallel decoding unit also receives an extrinsic parameter $L_{a,k}$ at the same time. The $L_{a,k}$ is the parameter that is obtained via a deinterleaving operation on the previous level extrinsic parameter $\Lambda(d_k)$. The initial value of the first level decoding unit extrinsic parameter is set as $L_{a0,k}=(0,0\ldots,0)$, a first level extrinsic parameter $L_{a1,k}$ is generated via the first level parallel decoding unit. And makes the message $r_{1s,k}$, $r_{1p,k}$ and $r_{2p,k}$ pass through sequentially to be the input of next level.

[0010] The turbo-code decoder mentioned above, wherein, the parallel decoding unit comprises a first decoder, a second decoder, an interleaving unit, and a deinterleaving unit. Wherein, the first decoder receives the $r_{1s,k}$, $r_{1p,k}$ messages and the extrinsic parameter $L_{a,k}$. The second decoder receives the $r_{2p,k}$ message and the extrinsic parameter $L_{a,k}$. The interleaving unit is allocated between the first decoder and the second decoder, receives the output of the first decoder. The deinterleaving unit is connected to the second decoder, alternately outputs the output of the first decoder and the second decoder.

[0011] The turbo-code decoder mentioned above, wherein, the first decoder of the parallel decoding units constitutes a systolic array VLSI circuits structure.

[0012] The turbo-code decoder mentioned above, wherein, the systolic array VLSI circuits is composed of N+M units of the module C, A, B, D, and E. Wherein, the module C receives $L_{a1,k}$, $r_{1s,k}$ and $r_{1p,k}$, and outputs $r_k^{(1)}(m)$ and $r_k^{(0)}(m)$. Module A calculates a forward recursive probability parameter α_k. Module B calculates a backward recursive probability parameter β_k. Module D adopts (N+M) units of parallel calculation to obtain the $\Lambda(d_k)$ after the calculation of the α_k, β_k, and $\gamma_k^{(i)}$ are finished. Module E outputs the value of the calculation from the module D, K=0, 1, …, N+M-1.

[0013] The turbo-code decoder mentioned above, wherein, the value of the $\Lambda(d_k)$ is calculated according to a MAP algorithm and following equation:

$$\Lambda(d_k) = \log \frac{\sum_m \sum_{m'} \gamma_k^{(1)}(m',m) \cdot \alpha_{k-1}(m') \cdot \beta_k(m)}{\sum_m \sum_{m'} \gamma_k^{(0)}(m',m) \cdot \alpha_{k-1}(m') \cdot \beta_k(m)}$$

[0014] Wherein, α_{k} is the forward recursive probability parameter, β_{k} is the backward recursive probability parameter, $\gamma_k^{(i)}$ is a branch probability parameter.

[0015] The turbo-code decoder mentioned above, wherein, the forward recursive probability parameter α_{k} is obtained from the calculation of the previous parameter α_{k-1} and the branch probability parameter $\gamma_k^{(i)}$, the equation is as follows:

$$\alpha_k(m) = \frac{\sum_{m'} \sum_{i=0}^{1} \gamma^{(i)}_k(m',m) \cdot \alpha_{k-1}(m')}{\sum_{m} \sum_{m'} \sum_{i=0}^{1} \gamma_k^{(i)}(m',m) \cdot \alpha_{k-1}(m')}$$

[0016] The turbo-code decoder mentioned above, wherein, the backward recursive probability parameter β_{k} is obtained from the calculation of the next parameter β_{k+1} and the branch probability parameter $\gamma_k^{(i)}$, the equation is as follows:

$$\beta_k(m) = \frac{\sum_{m'} \sum_{i=0}^{1} \gamma_{k+1}^{(i)}(m',m) \cdot \beta_{k+1}(m')}{\sum_{m} \sum_{m'} \sum_{i=0}^{1} \gamma_{k+1}^{(i)}(m',m) \cdot \beta_{k+1}(m')}$$

[0017] The turbo-code decoder mentioned above, wherein, the branch probability parameter $\gamma_k^{(i)}$ is obtained from following equation according to the MAP algorithm:

$$\gamma_k^{(i)}(m',m) = p(\gamma_{1s,k} \mid d_k = i, s_k = m, s_{k-1} = m') \cdot p(r_{1s,k} \mid d_k = i, s_k = m, s_{k-1} = m') \cdot \\ q(d_k = i \mid s_k = m, s_{k-1} = m') \cdot \Pr\{s_k = m \mid s_{k-1} = m'\}$$

[0018] Wherein whether the probability parameter $q(d_k = i \mid s_k = m, s_{k-1} = m')$ is 0 or 1 depends on the input bit $d_k = i$ is 0 or 1 combines the probability of the state m' to the state m.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention. In the drawings,

[0020] FIG. 1 schematically shows a turbo-code encoder comprising of two parallel RSC encoders;

[0021] FIG. 2 schematically shows the decoding structure of the turbo-code;

[0022] FIG. 3 schematically shows the structure of the P levels parallel decoding unit (Level 1, Level 2, ..., Level P);

[0023] FIG. 4 schematically shows the structure of the first level decoding unit of the parallel decoding units in FIG. 3;

[0024] FIG. 5 schematically shows the structure of the systolic array VLSI that is composed of the first level decoding unit of the parallel decoding unit in FIG. 4;

[0025] FIG. 6 schematically shows the structure of the simplified modules, data streams, and the latches of the parallel decoding units in FIG. 3 when N=4 and M=3;

[0026] FIG. 7 schematically shows the calculation structure of the branch probability parameter $\gamma_k^{(i)}(m',m)$;

[0027] FIG. 8 schematically shows the structure of module A for calculating α_k;

[0028] FIG. 9 schematically shows the structure of module B for calculating β_k;

[0029] FIG. 10 schematically shows the structure of module D for calculating $\Lambda(d_k)$;

[0030] FIG. 11 schematically shows the structure of the calculation submodule L (using analog circuit);

[0031] FIG. 12 schematically shows the structure of the fast RSC encoder, wherein, G_b=1011, G_d=1110;

[0032] FIG. 13 schematically shows the trellis diagram;

[0033] FIG. 14 schematically shows the detail structure of module A (wherein the submodule L is designed as the digital circuit);

[0034] FIG. 15 schematically shows the detail structure of module D;

[0035] FIG. 16 schematically shows the latency for accomplishing a message having a block size length; and

[0036] FIG. 17 schematically shows the comparison of the bit error rate, wherein, the iterative decoding number P=6, code ratio R=1/3, register size M=3, generator parameter G_b=1011, G_d=1110, the 256*256 random interleaving method is adopted by the first decoder and the second decoder.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0037] The present invention provides a structure design adopting the parallel and systolic array VLSI. The structure design adopting the parallel and systolic array VLSI mentioned above, wherein the decoder is designed to use the systolic array VLSI circuits. Since the output of previous level can be used as the input of next level. So the advantages of the parallel and the pipeline calculation are totally achieved. The latency is only N+M+2 units of time, the latency is shorten to as about 1/5 comparing to the conventional sequential calculation structure that takes 5*(N+M) units of time. The decoding throughput is about 5*(N+M) times higher than the conventional decoder. Although the quantity of the circuit gate is about 5*(N+M) times higher than the conventional decoder. However, the VLSI techniques had been progressively improved nowadays, thus the hardware complexity is easy to overcome. Devoting the hardware cost to get the higher speed will be a changeless trend.

[0038] Berrou, Glavieux and Thitimajshima first proposed the turbo-code whose error-correcting capability nears to the Shannon limited error-correcting in 1993 (C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon Limited Error-correcting Coding and Decoding: Turbo-codes (1)," in Proc. ICC'93, May, 1993). The encoding structure comprises two parallel recursive systematic convolution encoder (hereafter abbreviated as RSC). The important characteristics are (1) Two convolution codes with the same structure encode in parallel, thus the receiving end is able to decode the message repeatedly; (2) To increase the minimum distance between two encoding codes by using the non-uniform random interleaving (S. Benedetto and G. Montorsi: "Role of Recursive Convolutional Codes in Turbo Codes," Electron. Lett., Vol.31, No.11, pp. 858-859, 1995); and (3) Soft-in Soft-out decoding.

[0039] Because the characteristics mentioned above, the capability of the error-correcting appears equal and excellent. Due to the excellence of the error-correcting capability, the turbo-code is widely applied in the general communication system such as the CDMA transmission system (J. Blaanz, P. Jung, and M. Na B han, "Realistic Simulations of CDMA Mobile Radio Systems Using Joint Detection and Coherent Receiver Antenna Diversity," IEEE third International Symposium on Spread Spectrum Techniques and Applications, Oulu Finland, 1994).

[0040] Referring to FIG. 1, it schematically shows a turbo-code encoder comprising of two parallel RSC encoders. The input bit sequence is represented as $d=(d_1, d_2, d_3, \ldots\ldots, d_k , \ldots, d_N)$, where d_k is the input bit of the encoder at time k, k is from 1 to N, N is the block size. The output of the encoder at time k is represented as $c_k=(x_k,y_{1k},y_{2k})$. Since the encoder is systematic, so $x_k = d_k$, the surplus code output is represented as y_{1k},y_{2k}. The decoding structure of the turbo-code is shown in FIG. 2. The decoder 200 comprises two recursive decoding units 210 and 220; two recursive decoding units 210 and 220 are connected in interleaving and deinterleaving unit as shown as the 212, 214 and 216 in the diagram.

[0041] It is assuming that the Gaussian noise is the noise used in the communication channel. It is further assuming that the noise of each transmission symbol is an independent noise, the expectation value is 0, and the variant is $N_0/2$. Using the binary modulation, if the input bit d_k is 0, the modulation is –1.0; if the input bit d_k is 1, the modulation is +1.0. Therefore, the sequence of the receiving vector R is represented as $R=(r_1, r_2, r_3, \ldots\ldots, r_k, \ldots, r_N)$, the kth symbol is represented as

$$r_k = (r_{1s,k}, r_{1p,k}, r_{2p,k}) = (2x_k-1+n_{1s,k}, 2y_{1k}-1+n_{1p,k}, 2y_{2k}-1+n_{2p,k})$$

[0042] Wherein, $n_{1s,k}$, $n_{1p,k}$, and $n_{2p,k}$ is the noise of the channel r_{1s}, r_{1p}, r_{2p} at time k respectively, and they are independent each other. The detail of the Maximum A Posteriori (hereafter abbreviated as MAP) algorithm proposed by BCJR (L. Bahl, J. Cocke, F. Jelinek, and J. Raviv, "Optimal Decoding of Linear Codes for Minimizing Symbol Error Rate," IEEE Tran. I. T., Vol.20, pp.284-287, March 1974) is not superfluously described here. Herein, only describe the result of the MAP algorithm. The objective of the MAP algorithm is to calculate whether the A Posterioi Probability (hereafter abbreviated as APP) of each input bit d_k is the ratio of 1 or 0. Wherein, $k=0, 1, 2, \ldots, N-1$. From the derivation result of the turbo-code having the error-correcting capability nears to the Shannon limited error-correcting proposed by Berrou, Glavieux and Thitimajshima mentioned above, the following equation is obtained:

$$\Lambda(d_k) = \log \frac{\sum_m \sum_{m'} \gamma_k^{(1)}(m',m) \cdot \alpha_{k-1}(m') \cdot \beta_k(m)}{\sum_m \sum_{m'} \gamma_k^{(0)}(m',m) \cdot \alpha_{k-1}(m') \cdot \beta_k(m)} \qquad (1)$$

Wherein, α_k is the forward recursive probability parameter, β_k is the backward recursive probability parameter, $\gamma_k^{(i)}$ is the branch probability parameter. As we can see from the name, the forward recursive probability parameter α_k can be obtained from the calculation of the previous parameter α_{k-1} and the branch probability parameter $\gamma_k^{(i)}$, the equation is as follows:

$$\alpha_k(m) = \frac{\sum_{m'} \sum_{i=0}^{1} \gamma_k^{(i)}(m',m) \cdot \alpha_{k-1}(m')}{\sum_m \sum_{m'} \sum_{i=0}^{1} \gamma_k^{(i)}(m',m) \cdot \alpha_{k-1}(m')} \qquad (2)$$

The backward recursive probability parameter β_k can be obtained from the calculation of the next parameter β_{k+1} and the branch probability parameter $\gamma_{k+1}^{(i)}$, the equation is as follows:

$$\beta_k(m) = \frac{\sum_{m'} \sum_{i=0}^{1} \gamma_{k+1}^{(i)}(m',m) \cdot \beta_{k+1}(m')}{\sum_m \sum_{m'} \sum_{i=0}^{1} \gamma_{k+1}^{(i)}(m',m) \cdot \beta_{k+1}(m')} \qquad (3)$$

The branch probability parameter $\gamma_k^{(i)}$ is obtained from following equation according to the MAP algorithm:

$$\begin{aligned} &\gamma_k^{(i)}(m',m) = p(\gamma_{1s,k} \mid d_k = i, s_k = m, s_{k-1} = m') \cdot p(r_{1s,k} \mid d_k = i, s_k = m, s_{k-1} = m') \cdot \\ &q(d_k = i \mid s_k = m, s_{k-1} = m') \cdot \Pr\{s_k = m \mid s_{k-1} = m'\} \end{aligned} \qquad (4)$$

Wherein, whether the probability parameter $q(d_k = i \mid s_k = m, s_{k-1} = m')$ is 0 or 1 depends on the input bit $d_k = i$ is 0 or 1 combines the probability of the state m' to the state m.

[0043] In a sequential calculation decoder, it is assuming that each $\Lambda(d_k)$ in equation (1) needs a unit of time, wherein, K is from 0 to N+M-1, N stands for the block length of the transmission, and M stands for the register size of the decoder. It is further assuming that α_{k}, β_{k}, and $\gamma_k^{(i)}$ in equation (2), (3), and (4) needs a unit of time respectively, wherein, i=0 or 1. Therefore, the first level decoder needs 5*(N+M) units of time. According to the decoding algorithm such as the Viterbi algorithm (A.J. Viterbi, "Error Bound for Convolutional Codes and an Asymptotically Optimum Decoding Algorithm," IEEE Trans. Inform. Theorem, vol.IT-13, pp.260-269 Apr. 1967)(A.J. Viterbi and J.K. Omura, "Principles of digital communication and coding," New York: MacGraw-Hill, 1979) or the BCJR algorithm mentioned above, if N is too small, the error-correcting capability is not good. However, if N is too big, for a communication system needs the real time processing, the decoding delay is too big to tolerant.

[0044] As mentioned in the previous paragraph, currently the decoding algorithm is used to decide the value of $\Lambda(d_k)$ in equation (1), if $\Lambda(d_k)$>0, d_k=1, otherwise, d_k=0. To calculate each $\Lambda(d_k)$ in equation (1), the α_{k}, β_{k}, and $\gamma_k^{(i)}$ in equation (2), (3), and (4) must be calculated first. For a sequential calculation decoder, it needs 5*(N+M) units of time (G.Masera, G. Piccinini, M.R. Roch, nad M. Zqmboni, "VLSI Architectures for Turbo Codes," IEEE Trans. On VLSI Systems, vol.7, no.3, pp. 369-379, Sep.1999).

[0045] In order to increase the calculation speed and thus to increase the throughput. A preferred embodiment of the present invention adopts the parallel and systolic array VLSI structure design. The whole decoder circuit is composed of P levels parallel decoding units. The structure is shown in FIG. 3. There is a serial in parallel out unit before the first level to receive the message $r_{1s,k}$, $r_{1p,k}$, and $r_{2p,k}$, wherein, the subscript K=0,1,...,N+M-1 represents the whole block and end message. The output is sent to the first level decoding unit, the other input of the first level decoding unit is $L_{a,k}$, herein, the $L_{a,k}$ is the parameter obtained via the deinterleaving on the previous level extrinsic parameter $\Lambda(d_k)$, the initial value of the 0th level decoding unit extrinsic parameter is set as $L_{a0,k}$=(0,0...,0). The first level extrinsic parameter $L_{a1,k}$ is generated via the first level decoding unit, and the message $r_{1s,k}$, $r_{1p,k}$, and $r_{2p,k}$ sequentially pass through to be the input of next level.

[0046] Each level of the decoding unit comprises two decoders. These two decoders are the first decoder and the second decoder as shown in FIG. 4, wherein, the structure of the first decoder is similar to the second decoder's. The whole systolic array VLSI structure is shown in FIG. 5. Wherein, N and M can be adjusted according to the design requirement. For easy to describe, the block length N=4 and register size M=3 are used as an example. FIG. 6 schematically shows the structure of the simplified modules, data streams, and the latches. It is apparent for those who skilled in the art that even the embodiment is used as an example in the present invention, the embodiment will not limit the apply range of the present invention.

[0047] According to the literature (I.L. Turner, "A Modified BAHL Algorithm for Recursive System Convolutional Codes on Rayleigh Fading Channels," IEEE 49th Vehicular Technology Conference, pp.75-76 vol.1, 1999), the apriori probability of the input bit d_k calculated by the previous level decoder is represented as

$$\Pr\{s_k = m \mid s_{k-1} = m\} = \frac{e^{L(d_K)}}{1+e^{L(d_K)}}\ \text{, if } q(d_k=1 \mid s_k=m, s_{k-1}=m')=1 \qquad (5)$$

$$\Pr\{s_k = m \mid s_{k-1} = m\} = \frac{e^{L(d_K)}}{1+e^{L(d_K)}} = \frac{1}{1+e^{L(d_K)}}\text{, if } q(d_k=0 \mid s_k=m, s_{k-1}=m')=1 \qquad (6)$$

Wherein, $\mathrm{L}(\mathrm{d}_{\mathrm{k}})$ is the log likelihood ratio (LLR) extrinsic parameter calculated from the message bit d_{k} by the previous level decoder. It is assumed in a AWGN channel, well than, the partial probability of the equation (4) is calculated as follows:

$$p(r_{1s,k} \mid d_k = i, s_k = m, s_{k-1} = m') = \frac{1}{\sqrt{2\pi}\sigma_{r1s}} \exp\left[\frac{-(r_{1s,k} - \mu_{r1s})^2}{2\sigma_{r1s}^2}\right] \qquad (7)$$

$$p(r_{1p,k} \mid d_k = i, s_k = m, s_{k-1} = m') = \frac{1}{\sqrt{2\pi}\sigma_{r1p}} \exp\left[\frac{-(r_{1p,k} - \mu_{r1p}(m',m))^2}{2\sigma_{r1p}^2}\right] \qquad (8)$$

Wherein, μ_{r1s} and $\mu_{r1p}(m',m)$ is the expectation value of r_{1s} and r_{1p} respectively. Thereinto, μ_{r1s} depends on the input bit, and $\mu_{r1p}(m',m)$ depends on the input bit and also impacted by the previous state and current state. σ_{rls}^2 and σ_{rlp}^2 is the variant of the r_{ls} and r_{lp} respectively. It is assumed that the variant of r_{ls} and r_{lp} are the same. Therefore, the above two equations can be multiplied and consolidated as follows:

$$\begin{aligned} & p(r_{1s,k} \mid d_k = i, s_k = m, s_{k-1} = m') \cdot p(r_{1p,k} \mid d_k = i, s_k = m, s_{k-1} = m') \\ & = \frac{1}{2\pi\sigma^2} \exp\left[\frac{-1}{2} \cdot \frac{(r_{1s,k} - \mu_{r1s})^2 + (r_{1p,k} - \mu_{r1p}(m',m))^2}{\sigma^2}\right] \end{aligned} \qquad (9)$$

For a discrete memory-less gauss channel, the branch probability parameter γ_k^1 or γ_k^0 for input bit is 1 or 0 can be calculated from the equation (4), (5), (6), and (9) as follows:

$$\gamma_k^{(1)}(m',m) = \frac{1}{2\pi\sigma^2} \exp\left[\frac{-1}{2} \cdot \frac{(r_{1s,k} - 1)^2 + (r_{1p,k} - \mu_{r1p}(m',m))^2}{\sigma^2}\right] \bullet \frac{e^{L(d_K)}}{1 + e^{L(d_K)}} \qquad (10)$$

$$\gamma_k^{(0)}(m',m) = \frac{1}{2\pi\sigma^2} \exp\left[\frac{-1}{2} \cdot \frac{(r_{1s,k} + 1)^2 + (r_{1p,k} - \mu_{r1p}(m',m))^2}{\sigma^2}\right] \bullet \frac{1}{1 + e^{L(d_K)}} \qquad (11)$$

[0048] According to the equation (10) and (11), the branch probability parameter $\gamma_k^{(i)}(m',m)$ can be calculated in parallel. The N+M units of the module C (as shown in FIG. 7) are used to calculate each $\gamma_k^{(i)}(m',m)$ in parallel. Thus, the N+M units of time can be shortened to a unit of time. The input signal of the module C in FIG. 7 is $L_{a,k}$, $r_{1s,k}$ and $r_{1p,k}$ respectively, wherein, $k=1,\ldots,N+M$. The module C is used to calculate $\gamma_k^{(1)}(m',m)$ and $\gamma_k^{(0)}(m',m)$ respectively.

[0049] In addition, since the forward recursive probability parameter α_k is output from the previous level to be the input of the next level, and the backward recursive probability parameter β_k is output from the next level to be the input of the previous level. It is suitable to design as the systolic array VLSI to increase the calculation speed. According to the equation (2), N+M units of Module A (as shown in FIG. 8) are used to calculate α_k. Wherein, the first level input is $\gamma_1^{(1)}(m',m)$ and $\gamma_1^{(0)}(m',m)$ and the initial value of the forward recursive probability parameter $\alpha_0(m)$ are used to calculate $\alpha_1(m)$. The second level input $\gamma_2^{(1)}(m',m)$ and $\gamma_2^{(0)}(m',m)$ and $\alpha_1(m)$ are used to calculate $\alpha_2(m)$. Thus, the systolic array is able to work simultaneously. All $\alpha_k(m)$, wherein $k=1\ldots,N-M$, can be calculated after N+M units of time.

[0050] According to the equation (3), it adopts N+M units of Module B (as shown in FIG. 9) for calculating β_k. Wherein, the first level input is $\gamma_{N+M}^{(1)}(m',m)$ and $\gamma_{N+M}^{(0)}(m',m)$ and the initial value of the backward recursive probability parameter $\beta_{N+M}(m)$ are used to calculate $\beta_{N+M-1}(m)$. The inputs of the second level $\gamma_{N+M-1}^{(1)}(m',m)$ and $\gamma_{N+M-1}^{(0)}(m',m)$, and the backward recursive probability parameter $\beta_{N+M-1}(m)$ are used to calculate $\beta_{N+M-2}(m)$. The advantage is the structure of each module is the same; the output of the previous level is the input of the next level. Thus, the throughput is (N+M) times of the original throughput.

[0051] When the calculation of α_{k}, β_{k} and $\gamma_k^{(i)}$ are completed, according to the equation (1), it adopts N+M units of module D (as the module D shown in FIG. 10) to calculate $\Lambda(d_k)$. By using the parallel calculation, the N+M units of time is shortened to a unit of time.

[0052] The submodule L located in between the module A and the module B calculates the product-sum of two inputs. As the example shown in FIG. 11, the submodule L adopts the analog circuit provided by the conventional technique. The analog circuits proposed by the reference literatures also can be used. Like H.-A.Loeliger, F. Lustenberger, F. Tarkoy, M. Helfensten, "Decoding in Analog VLSI," IEEE Communication Magzine, Vol.37 (4), pp.99-101 Apr. 1999, or H.-A.Loeliger, F. Lustenberger, M. Helfensten, F. Tarkoy, "Probability Propagation and Decoding in Analog VLSI," IEEE Trans.on Information Theory, Vol.47(2), pp.837-843 Feb. 2001, or F. Lustenberger, M. Helfenstein, H,-A, Loeliger, F. Tarkoy, G.S. Moschytz, "An Analog VLSI Decoding Technique for Digital Codes," ISCAS '99. Proceedings of the 1999 IEEE international Symposium on Circuits and Systems, Vol. 2, pp.424-427 1999,..., etc.

[0053] For easy to describe the detail structure of the module A, B, and D mentioned above, the preferred embodiment of the present invention uses the turbo-code of the third generation CDMA mobile communication standard as an example for description. However, it is not used to limit the apply range of the present invention. The turbo-code of the third generation CDMA mobile communication standard is: a decoder register size M=3. For the first decoder and the second decoder, the code ratio R=1/3, the parameter of the feedback generator and the parameter of the direct-feed-forward generator is G_b=1011 and G_d=1110respectively. As shown in FIG. 12, the recursive systematic convolution encoder (hereafter abbreviated as RSC), wherein, the RSC adopts the fast

RSC encoder, for the physical content of the fast RSC encoder, please refer to the "Fast Turbo-code Encoder" proposed by the same inventor of the present invention in April, 2001. The trellis diagram is shown in FIG. 13.

[0054] Referring to the content of FIG. 6, FIG. 6 schematically shows the structure of the simplified modules, data streams, and the latches when the block length N=4 and the register size M=3. There are N+M=7 units of the module A, B, C, and D. In the first unit of time, the parallel input $L_{a,k}$, $r_{1s,k}$ and $r_{1p,k}$ signals, k=1,2,...,6,7 are used simultaneously to calculate the $\gamma_1^{(i)}$, $\gamma_2^{(i)}$, ..., $\gamma_7^{(i)}$. In the 7 units of time afterwards, the α_1, α_2,..., α_6 and β_1, β_2, ..., β_6 is calculated respectively. In the other one unit of time afterwards, according to the equation (2), the parallel input $\gamma_k^{(1)}(m',m)$, $\gamma_k^{(0)}(m',m)$, α_{k-1} and β_{k-1} are used to calculate $\Lambda(d_k)$. The $\Lambda(d_k)$ is used as the extrinsic parameter of the next level, if the last level is reached, the d_k is determined accordingly, if d_k>0, determine d_k =1, otherwise d_k=0.

[0055] According to the trellis diagram of FIG. 13. It is easy to simplify the structure of the module A, B, and D. FIG. 14 schematically shows the detail structure of the module A based on this design. The detail structure of the module B is also similar to the module A. The detail structure of the module D is shown in FIG. 15.

[0056] The latency spent for accomplishing a message with one block size length of the parallel and systolic array VLSI structure design of the preferred embodiment according to the present invention, as shown in FIG. 16, is N+M+2 units of time. Comparing to the original conventional sequential calculation structure that needs 5*(N+M) units of time, the time is shortened to about 1/5 only. Furthermore, the systolic array VLSI structure design is able to generate a set of d_k in every one unit of time after the first set of d_k is generated.

The performance comparison is shown in table 1:

Table 1: The structure comparison of the systolic array and the sequential type

Item/Structure	Sequential Structure	Systolic Array Structure	Pro and Con
Latency	5*(N+M)	(N+M)+2	The latency is about 1/5
Output Time	5*(N+M)	1	The throughput is about 5*(N+M) times
Number of Hardware Gate	1	5*(N+M)	The complexity of the circuit is about 5*(N+M) times

[0057] In order to prove the error-correcting feature of the preferred embodiment according to the present invention. Herein, the CDMA mobile communication system mentioned above is used as an example. The RSC decoder with register size M=3 is shown in FIG. 12. The trellis diagram is shown in FIG. 13. The iterative decoding number P=6. The random interleaving method is adopted in between the first decoder and the second decoder. The simulation result is obtained as shown in FIG. 17, wherein, the block length N=65536, the vertical axis is the decoding performance denoted by the bit error rate (BER). The horizontal axis is the communication environment denoted by the signal/noise ratio. As we can see here, under the situation with the same signal/noise ratio, the larger the iterative decoding number, the better the decoding performance. This is accorded with the theory, and is similar to the simulation result disclosed in the contents of the literatures: C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon Limited Error-correcting Coding and Decoding: Turbo-codes (1)," in Proc. ICC'93, May, 1993, and P.Robertson "Illuminating the Structure of Code and Decoder of Parallel Concatenated Recursive Systmatic (Turbo) Codes," in Proc. IEEE GLOBECOM Conf., San Francisco, CA. Pp. 1298-1303, Dec.1994.

[0058] The present simulation uses the programming language C language running on the GenuineInter Pentium® III CPU,128 MB RAM personal computer. The simulation runs on the working platform with the Windows Me® operating system. The bit error rate comparison shown in FIG. 17, wherein, the iterative decoding number (p=1,...,6), the code ratio R=1/3, the register size M=3, the generator parameter G_b=1011, G_d=1110, and uses the 256*256 random interleaving deinterleaving method.

[0059] The present invention provides a fast turbo-code decoder. Wherein, the decoder is designed to use the systolic array VLSI circuits. Since the output of previous level can be used as the input of next level. So the advantages of the parallel and the pipeline calculation are totally achieved. The latency is only N+M+2 units of time, the latency is shorten to as about 1/5 comparing to the conventional sequential calculation structure that takes 5*(N+M) units of time. The decoding throughput is about 5*(N+M) times higher than the conventional decoder. Although the quantity of the circuit gate is about 5*(N+M) times higher than the conventional decoder. However, the VLSI techniques had been progressively improved nowadays, thus the hardware complexity is easy to overcome. Devoting the hardware cost to get the higher speed will be a changeless trend.

[0060] Although the invention has been described with reference to a particular embodiment thereof, it will be apparent to one of the ordinary skill in the art that modifications to the described embodiment may be made without departing from the spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed description.